



Winstar Display Co., LTD

華凌光電股份有限公司



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SPECIFICATION

CUSTOMER : _____

MODULE NO.: **WF57BTIBCDD#**

APPROVED BY: (FOR CUSTOMER USE ONLY)		
	PCB VERSION:	DATA:

SALES BY	APPROVED BY	CHECKED BY	PREPARED BY

VERSION	DATE	REVISED PAGE NO.	SUMMARY
B	2011.01.10	9~16	Correct DC Characteristics & AC Characteristics &Data transfer order Setting



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MODLE NO :

RECORDS OF REVISION

DOC. FIRST ISSUE

VERSION	DATE	REVISED PAGE NO.	SUMMARY
0	2009/5/13		First issue
A	2009/8/12	20	Modify LED Life Time
B	2011.01.10	9~16	Correct DC Characteristics & AC Characteristics &Data transfer order Setting

Contents

1. Module Classification Information
2. Block Diagram
3. Electrical Characteristics
4. Absolute Maximum Ratings
5. Interface Pin Function
6. DC CHARACTERISTICS
7. AC Characteristics
8. Data transfer order Setting
9. Register Depiction
10. OPTICAL CHARACTERISTIC
11. Contour Drawing
12. LED driving conditions
13. Reliability Test

1.Module Classification Information

W F 57 B T I B C D D #
 ① ② ③ ④ ⑤ ⑥ ⑦ ⑧ ⑨ ⑩ ⑪

- ① Brand : WINSTAR DISPLAY CORPORATION
- ② Display Type : H→Character Type, G→Graphic Type F→TFT Type
- ③ Display Size : 5.7" TFT
- ④ Model serials no.
- ⑤ Backlight Type : F→CCFL, White T→LED, White

- ⑥ LCD Polarize A→Reflective, N.T, 6:00 H→Transflective, W.T,6:00
 Type/ Temperature D→Reflective, N.T, 12:00 K→Transflective, W.T,12:00
 range/ View G→Reflective, W. T, 6:00 C→Transmissive, N.T,6:00
 direction J→Reflective, W. T, 12:00 F→Transmissive, N.T,12:00
 B→Transflective, N.T,6:00 I→Transmissive, W. T, 6:00
 E→Transflective, N.T.12:00 L→Transmissive, W.T,12:00
- ⑦ A: TFT LCD
 B: TFT+FR+CONTROL BOARD
 C: TFT+FR+A/D BOARD
 D:TFT+FR+A/D BOARD+CONTROL BOARD
- ⑧ Solution: A: 128160 B:320234 C:320240 D:480234
- ⑨ D: Digital A: Analog
- ⑩ Version
- ⑪ Special Code #:Fit in with ROHS directive regulations

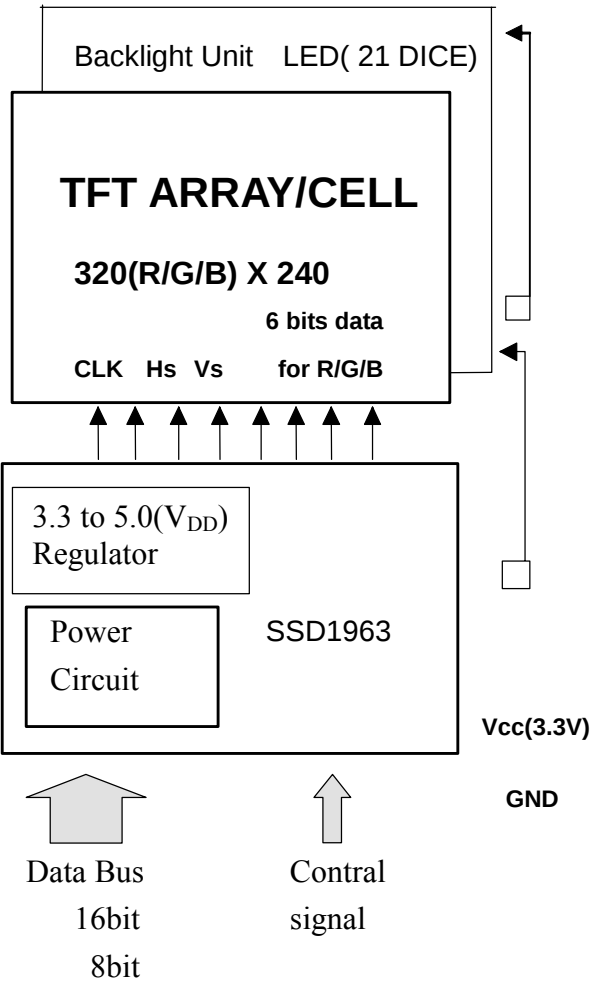
This product is composed of a TFT LCD panel, driver ICs, FPC, Control Board and a backlight unit. The following table described the features of WF57BTIBCDD#.

Item	Dimension	Unit
Dot Matrix	320 x RGBx240(TFT)	dots
Module dimension	149.0x 109.0 x 11.5 (max)	mm
View area	115.200x 86.40	mm
Dot pitch	0.12 x 0.36	mm
Driving IC package	COG	
LCD type	TFT, Negative, Transmissive	
View direction	6 o'clock	
Backlight Type	LED, Normally White	
Controller IC	SSD1963	

*Expose the IC number blaze (Luminosity over than 1 cd) when using the LCM may cause IC operating failure.

*Color tone slight changed by temperature and driving voltage.

2. Block Diagram



3.Electrical Characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage For Logic	VCC	—	3.0	3.3	3.6	V
Input High Volt.	V _{IH}	—	0.8VDD IO	—	VDDIO + 0.5	V
Input Low Volt.	V _{IL}	—	—	—	0.2VDDIO	V
LCD Driving Supply Voltage	V _{GH} *1	Ta=25°C		15		V *3
	V _{GL} *2			-10		V
	Vcom		—	3.7	—	
Supply Current	I _{VDD}	V _{DD} =3.3V	—	121	—	mA

Notes:

*1) VGH is TFT Gate on operating Voltage.

*2) VGL is TFT Gate off operating Voltage, VGL signal must be fluctuates with same phase as Vcom when Storage on Gate structure.

*3) Vcom must be adjusted to optimize display quality_Crosstalk, Contrast Ratio and etc.

4.Absolute Maximum Ratings

Item	Symbol	Min	Typ	Max	Unit
Operating Temperature	T _{OP}	-20	—	+70	°C
Storage Temperature	T _{ST}	-30	—	+80	°C
Power Supply Voltage	V _{GH}	-0.3	—	18	V
	V _{GL}	-15	—	0.3	V
	VCC	-0.3	—	6.0	V

5.Interface Pin Function

5-1 Pins Connection To Control Board

P/N	Symbol	16BIT Function	P/N	Symbol	16BIT Function
1	GND	Ground	26	RST	Reset
2	VCC	Power supply for Logic	27	RL	Scan direction
3	NC	No connection	28	UD	Scan direction
4	RS		29	NC	No connection
5	WR	8080 family MPU interface : Write signal	30	NC	No connection
6	RD	8080 family MPU interface: Read signal	31	NC	No connection
7	DB0	Data bus	32	NC	No connection
8	DB1				
9	DB2				
10	DB3				
11	DB4				
12	DB5				
13	DB6				
14	DB7				
15	DB8				
16	DB9				
17	DB10				
18	DB11				
19	DB12				
20	DB13				
21	DB14				
22	DB15				
23	NC	No connection			
24	NC	No connection			
25	CS	Chip select			

6. DC Characteristics

Conditions:

Voltage referenced to VSS

VDDD, VDDPLL = 1.2V

VDDIO, VDDLCD = 3.3V

TA = 25°C

DC Characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
PSTY	Quiescent Power			300	500	uW
IIZ	Input leakage current		-1		1	uA
IOZ	Output leakage current		-1		1	uA
VOH	Output high voltage		0.8VDDIO			V
VOL	Output low voltage				0.2VDDIO	V
VIH	Input high voltage		0.8VDDIO		VDDIO + 0.5	V
VIL	Input low voltage				0.2VDDIO	V

7. AC Characteristics

Conditions:

Voltage referenced to VSS

VDDD, VDDPLL = 1.2V

VDDIO, VDDLCD = 3.3V

TA = 25°C

CL = 50pF (Bus/CPU Interface)

CL = 0pF (LCD Panel Interface)

7.1 Clock Timing

Table 7-1: Clock Input Requirements for CLK (PLL-bypass)

Symbol	Parameter	Min	Max	Units
FCLK	Input Clock Frequency (CLK)		110	MHz
TCLK	Input Clock period (CLK)	1/fCLK		ns

Table 7-2: Clock Input Requirements for CLK

Symbol	Parameter	Min	Max	Units
FCLK	Input Clock Frequency (CLK)	2.5	50	MHz
TCLK	Input Clock period (CLK)	1/fCLK		ns

Table 7-3: Clock Input Requirements for crystal oscillator XTAL

Symbol	Parameter	Min	Max	Units
FXTAL	Input Clock Frequency	2.5	10	MHz
TXTAL	Input Clock period	1/fXTAL		ns

7.2 MCU Interface Timing

7.2.1 Parallel 6800-series Interface Timing

Table 7-4: Parallel 6800-series Interface Timing Characteristics (Use CS# as clock)

Symbol	Parameter	Min	Typ	Max	Unit																																																
fMCLK	System Clock Frequency*	1	-	110	MHz																																																
tMCLK	System Clock Period*	1/fMCLK	-	-	ns																																																
tPWCSH	Control Pulse High Width	Write Read	13 30	1.5* tMCLK 3.5* tMCLK	- ns																																																
tPWCSL	Control Pulse Low Width	Write (next write cycle) Write (next read cycle) Read	13 80 80	1.5* tMCLK 9* tMCLK 9* tMCLK	- ns																																																
tAS	Address Setup Time	2	-	-	ns																																																
tAH	Address Hold Time	2	-	-	ns																																																
tDSW	Data Setup Time	4	-	-	ns </tr <tr> <td>tDHW</td><td>Data Hold Time</td><td>1</td><td>-</td><td>-</td><td>ns</td></tr> <tr> <td>tPLW</td><td>Write Low Time</td><td>14</td><td>-</td><td>-</td><td>ns</td></tr> <tr> <td>tPHW</td><td>Write High Time</td><td>14</td><td>-</td><td>-</td><td>ns</td></tr> <tr> <td>tPLWR</td><td>Read Low Time</td><td>38</td><td>-</td><td>-</td><td>ns</td></tr> <tr> <td>tACC</td><td>Data Access Time</td><td>32</td><td>-</td><td>-</td><td>ns</td></tr> <tr> <td>tDHR</td><td>Output Hold time</td><td>1</td><td>-</td><td>-</td><td>ns</td></tr> <tr> <td>tR</td><td>Rise Time</td><td>-</td><td>-</td><td>0.5</td><td>ns</td></tr> <tr> <td>tF</td><td>Fall Time</td><td>-</td><td>-</td><td>0.5</td><td>ns</td></tr>	tDHW	Data Hold Time	1	-	-	ns	tPLW	Write Low Time	14	-	-	ns	tPHW	Write High Time	14	-	-	ns	tPLWR	Read Low Time	38	-	-	ns	tACC	Data Access Time	32	-	-	ns	tDHR	Output Hold time	1	-	-	ns	tR	Rise Time	-	-	0.5	ns	tF	Fall Time	-	-	0.5	ns
tDHW	Data Hold Time	1	-	-	ns																																																
tPLW	Write Low Time	14	-	-	ns																																																
tPHW	Write High Time	14	-	-	ns																																																
tPLWR	Read Low Time	38	-	-	ns																																																
tACC	Data Access Time	32	-	-	ns																																																
tDHR	Output Hold time	1	-	-	ns																																																
tR	Rise Time	-	-	0.5	ns																																																
tF	Fall Time	-	-	0.5	ns																																																

* System Clock denotes external input clock (PLL-bypass) or internal generated clock (PLL-enabled)

Figure 7-1: Parallel 6800-series Interface Timing Diagram (Use CS# as Clock)

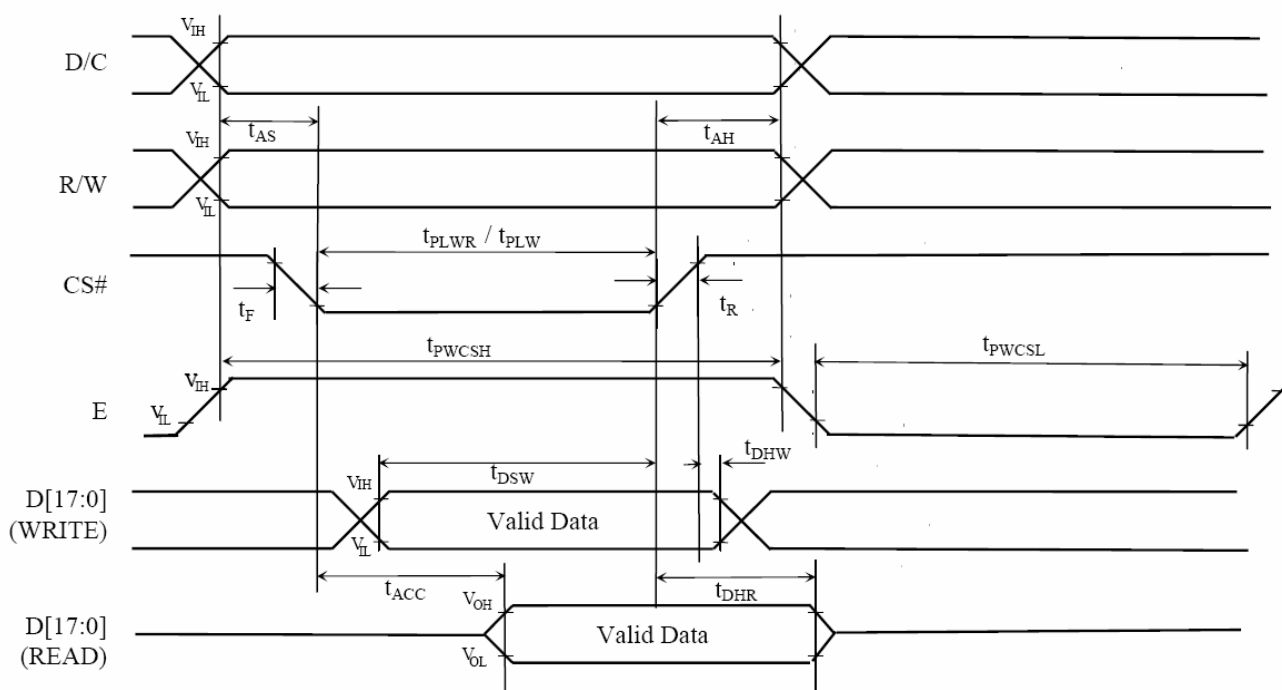
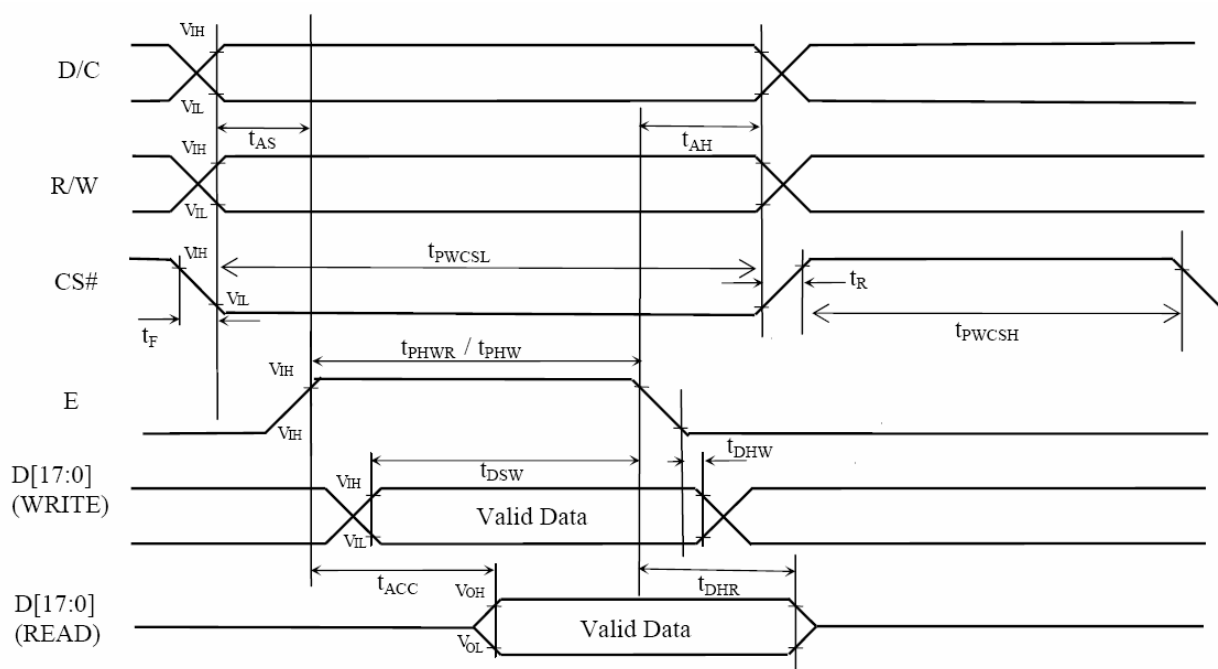


Table 7-5: Parallel 6800-series Interface Timing Characteristics (Use E as clock)

Symbol	Parameter	Min	Typ	Max	Unit
fMCLK	System Clock Frequency*	1	-	110	MHz
tMCLK	System Clock Period*	1/ fMCLK	-	-	ns
tPWCSH	Control Pulse Low Width	Write (next write cycle)	13	1.5* tMCLK	ns
		Write (next read cycle)	80	9* tMCLK	
		Read	80	9* tMCLK	
tPWCSL	Control Pulse High Width	Write	13	1.5* tMCLK	ns
		Read	30	3.5* tMCLK	
tAS	Address Setup Time	2	-	-	ns
tAH	Address Hold Time	2	-	-	ns
tDSW	Data Setup Time	4	-	-	ns
tDHW	Data Hold Time	1	-	-	ns
tPLW	Write Low Time	14	-	-	ns
tPHW	Write High Time	14	-	-	ns
tPLWR	Read Low Time	38	-	-	ns
tACC	Data Access Time	32	-	-	ns
tDHR	Output Hold time	1	-	-	ns
tR	Rise Time	-	-	0.5	ns
tF	Fall Time	-	-	0.5	ns

* System Clock denotes external input clock (PLL-bypass) or internal generated clock (PLL-enabled)

Figure7-2: Parallel 6800-series Interface Timing Diagram (Use E as Clock)



7.2.2 Parallel 8080-series Interface Timing

Table 7-6: Parallel 8080-series Interface

Symbol	Parameter		Min	Typ	Max	Unit
fMCLK	System Clock Frequency*		1	-	110	MHz
tMCLK	System Clock Period*		1/ fMCLK	-	-	ns
tPWCSL	Control Pulse High Width	Write Read	13 30	1.5* tMCLK 3.5* tMCLK	-	ns
tPWCSH	Control Pulse Low Width	Write (next write cycle) Write (next read cycle) Read	13 80 80	1.5* tMCLK 9* tMCLK 9* tMCLK	-	ns
tAS	Address Setup Time		1	-	-	ns
tAH	Address Hold Time		2	-	-	ns
tDSW	Write Data Setup Time		4	-	-	ns
tDHW	Write Data Hold Time		1	-	-	ns
tPWLW	Write Low Time		12	-	-	ns
tDHR	Read Data Hold Time		1	-	-	ns
tACC	Access Time		32	-	-	ns
tPWLR	Read Low Time		36	-	-	ns
tR	Rise Time		-	-	0.5	ns
tF	Fall Time		-	-	0.5	ns
tCS	Chip select setup time		2	-	-	ns
tCSH	Chip select hold time to read signal		3	-	-	ns

* System Clock denotes external input clock (PLL-bypass) or internal generated clock (PLL-enabled)

Figure 7-3: Parallel 8080-series Interface Timing Diagram (Write Cycle)

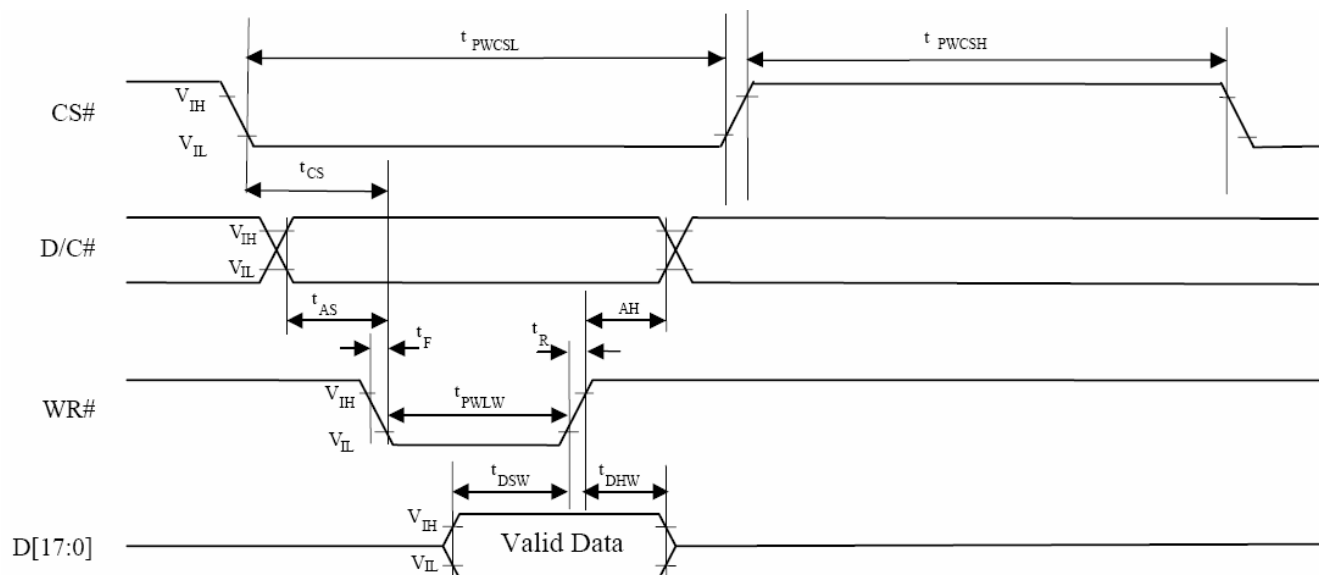
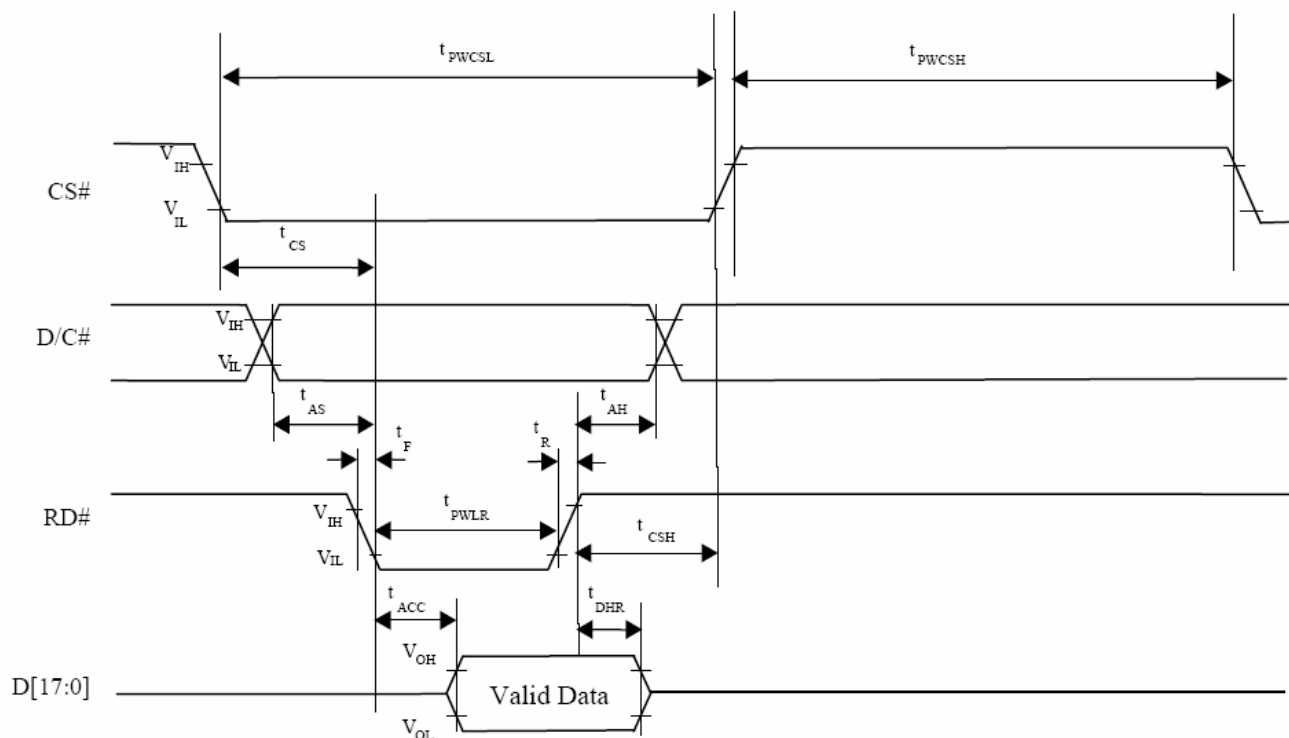


Figure 7-4: Parallel 8080-series Interface Timing Diagram (Read Cycle)



8. Data transfer order Setting

Pixel Data Format

Both 6800 and 8080 support 8-bit, 9-bit, 16-bit, 18-bit and 24-bit data bus. Depending on the width of the data bus, the display data are packed into the data bus in different ways.

Table 8-1: Pixel Data Format

Interface	Cycle	D[23]	D[22]	D[21]	D[20]	D[19]	D[18]	D[17]	D[16]	D[15]	D[14]	D[13]	D[12]	D[11]	D[10]	D[9]	D[8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
24 bits	1st	R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
18 bits	1st							R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
16 bits (565 format)	1st									R5	R4	R3	R2	R1	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1
16 bits	1st									R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0
	2nd									B7	B6	B5	B4	B3	B2	B1	B0	R7	R6	R5	R4	R3	R2	R1	R0
	3rd									G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
12 bits	1st													R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4
	2nd													G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
9 bits	1st																R5	R4	R3	R2	R1	R0	G5	G4	G3
	2nd																G2	G1	G0	B5	B4	B3	B2	B1	B0
8 bits	1st																	R7	R6	R5	R4	R3	R2	R1	R0
	2nd																	G7	G6	G5	G4	G3	G2	G1	G0
	3rd																	B7	B6	B5	B4	B3	B2	B1	B0

9 Register Depiction

Please consult the spec of SSD1963 Version 1.2

10. OPTICAL CHARATERISTIC

Ta=25±2℃, ILED=20mA

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response time		Tr	$\theta = 0^{\circ}$ 、 $\Phi = 0^{\circ}$	-	10		ms	Note 3,5
		Tf		-	15		ms	
Contrast ratio		CR	At optimized viewing angle	300	400	-	-	Note 4,5
Color Chromaticity	White	Wx	$\theta = 0^{\circ}$ 、 $\Phi = 0$	(0.26)	(0.31)	(0.36)		Note 2,6,7
		Wy		(0.28)	(0.33)	(0.38)		
	Red	Rx	$\theta = 0^{\circ}$ 、 $\Phi = 0$					
		Ry						
	Green	Gx	$\theta = 0^{\circ}$ 、 $\Phi = 0$					
		Gy						
	Blue	Bx	$\theta = 0^{\circ}$ 、 $\Phi = 0$					
		By						
Viewing angle	Hor.	Θ R	$CR \geq 10$	(50)	(60)		Deg.	Note 1
		Θ L		(50)	(60)			
	Ver.	Φ T		(40)	(50)			
		Φ B		(45)	(55)			
Brightness		-	-	200	250	-	cd/m ²	Center of display

Ta=25±2℃, IL=20mA

Note 1: Definition of viewing angle range

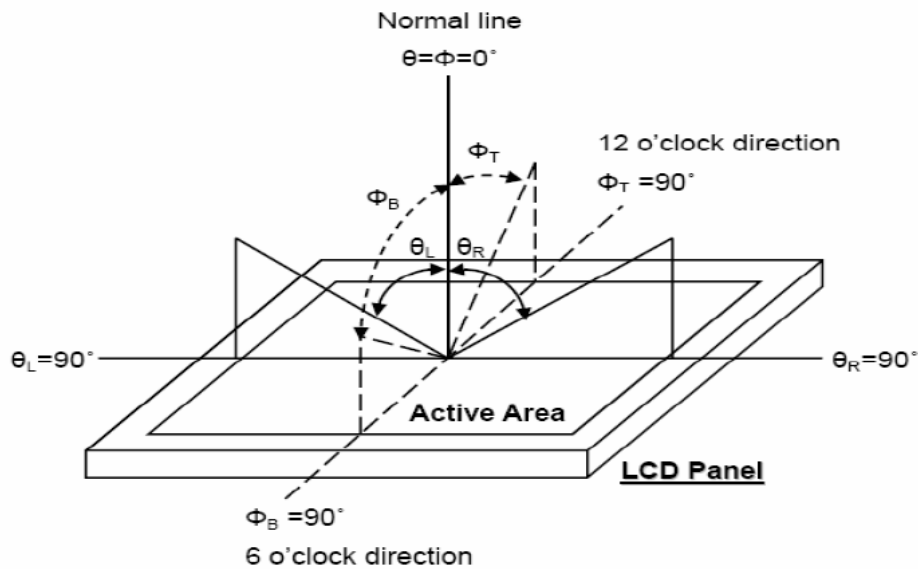


Fig. 8-1 Definition of viewing angle

Note 2: Test equipment setup:

After stabilizing and leaving the panel alone at a driven temperature for 10 minutes, the measurement should be executed. Measurement should be executed in a stable, windless, and dark room. Optical specifications are measured by Topcon BM-7 luminance meter 1.0° field of view at a distance of 50cm and normal direction.

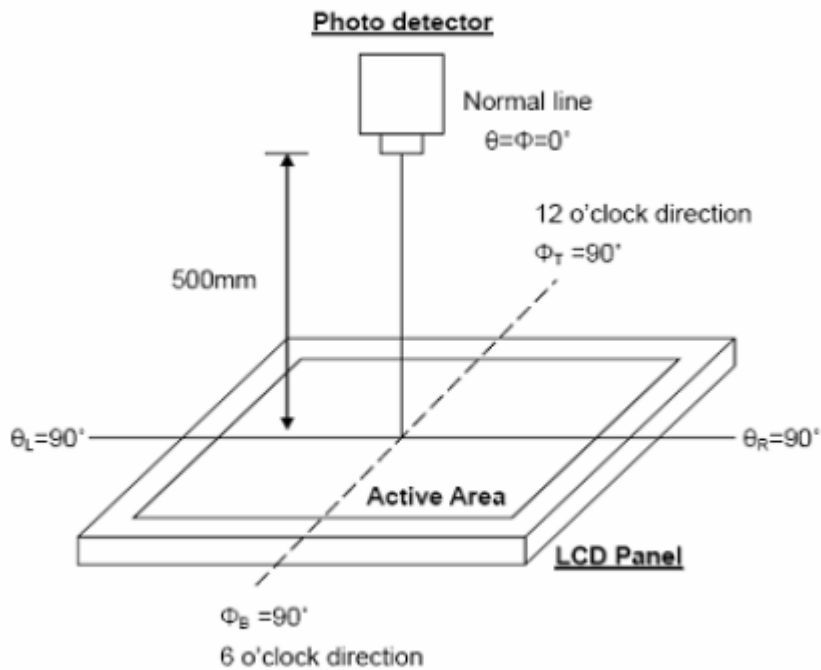


Fig. 8-2 Optical measurement system setup

Note 3: Definition of Response time:

The response time is defined as the LCD optical switching time interval between “White” state and “Black” state. Rise time, T_r , is the time between photo detector output intensity changed from 90% to 10% . And fall time, T_f , is the time between photo detector output intensity changed from 10% to 90% .

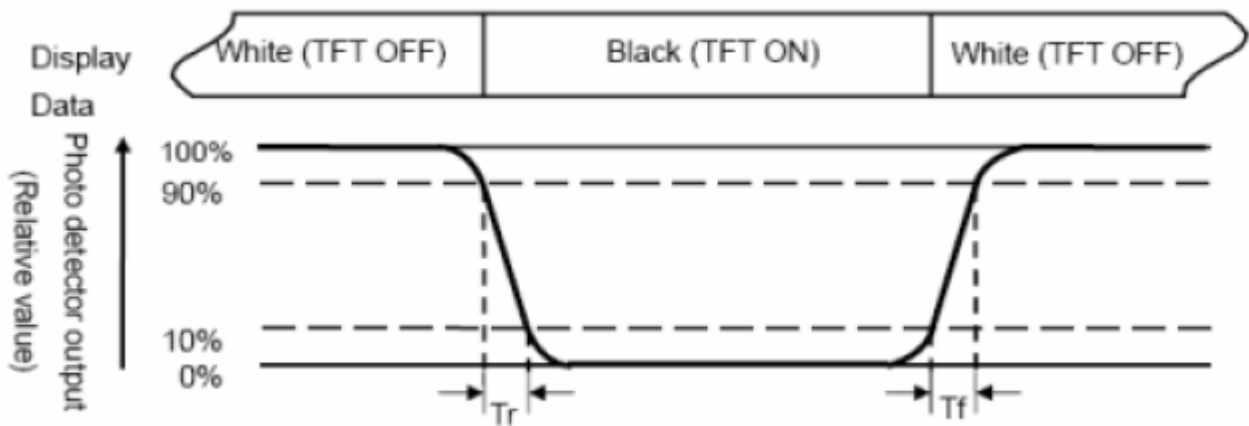


Fig. 3-3 Definition of response time

Note 4: Definition of contrast ratio:

The contrast ratio is defined as the following expression.

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD on the "White" state}}{\text{Luminance measured when LCD on the "Black" state}}$$

Note 5: White $V_i = V_{i50} \pm 1.5V$

Black $V_i = V_{i50} \pm 2.0V$

“ $\pm$ ” means that the analog input signal swings in phase with VCOM signal.

“ $\pm$ ” means that the analog input signal swings out of phase with VCOM signal.

The 100% transmission is defined as the transmission of LCD panel when all the input terminals of

module are electrically opened.

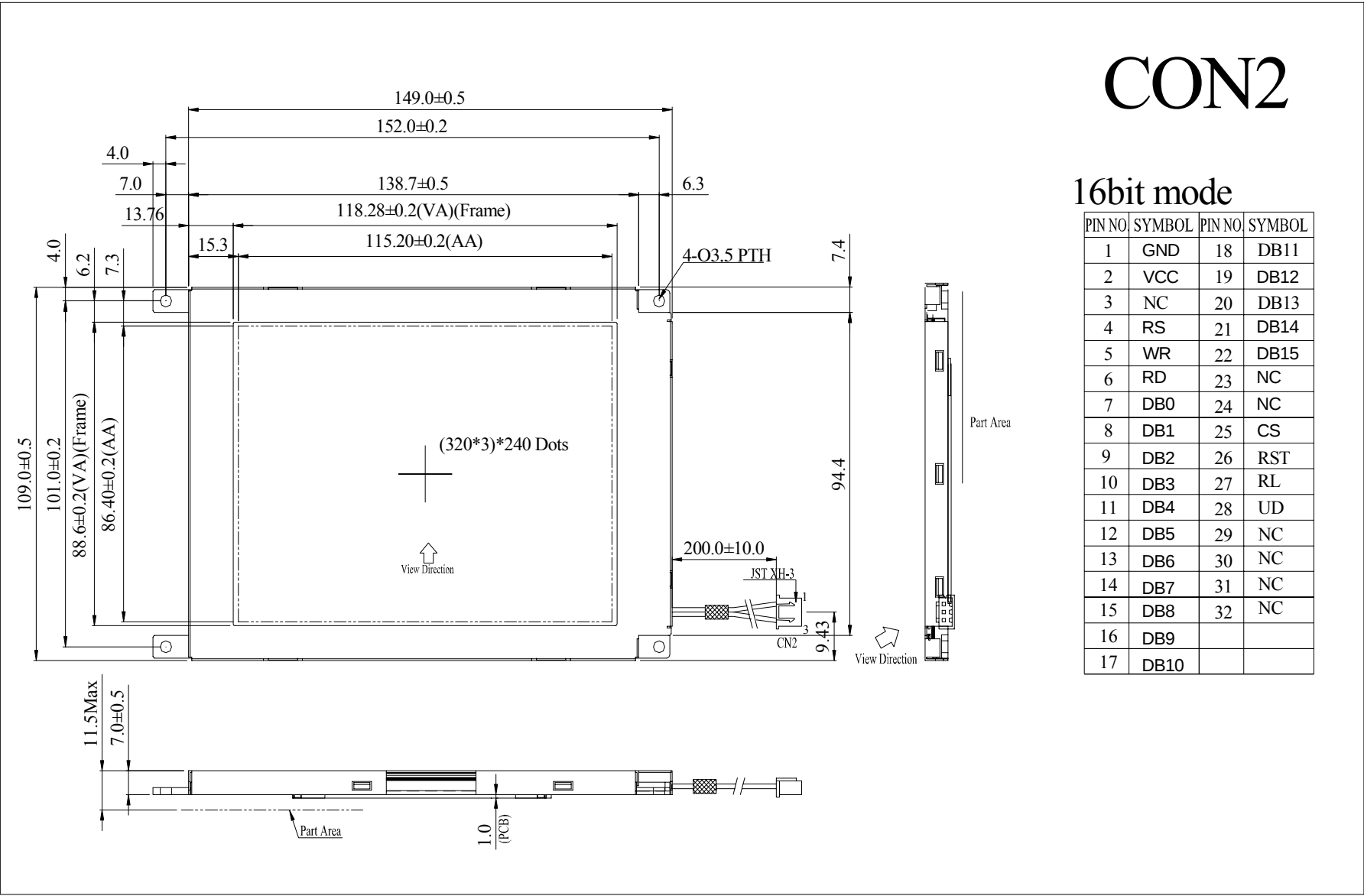
Note 6: Definition of color chromaticity (CIE 1931)

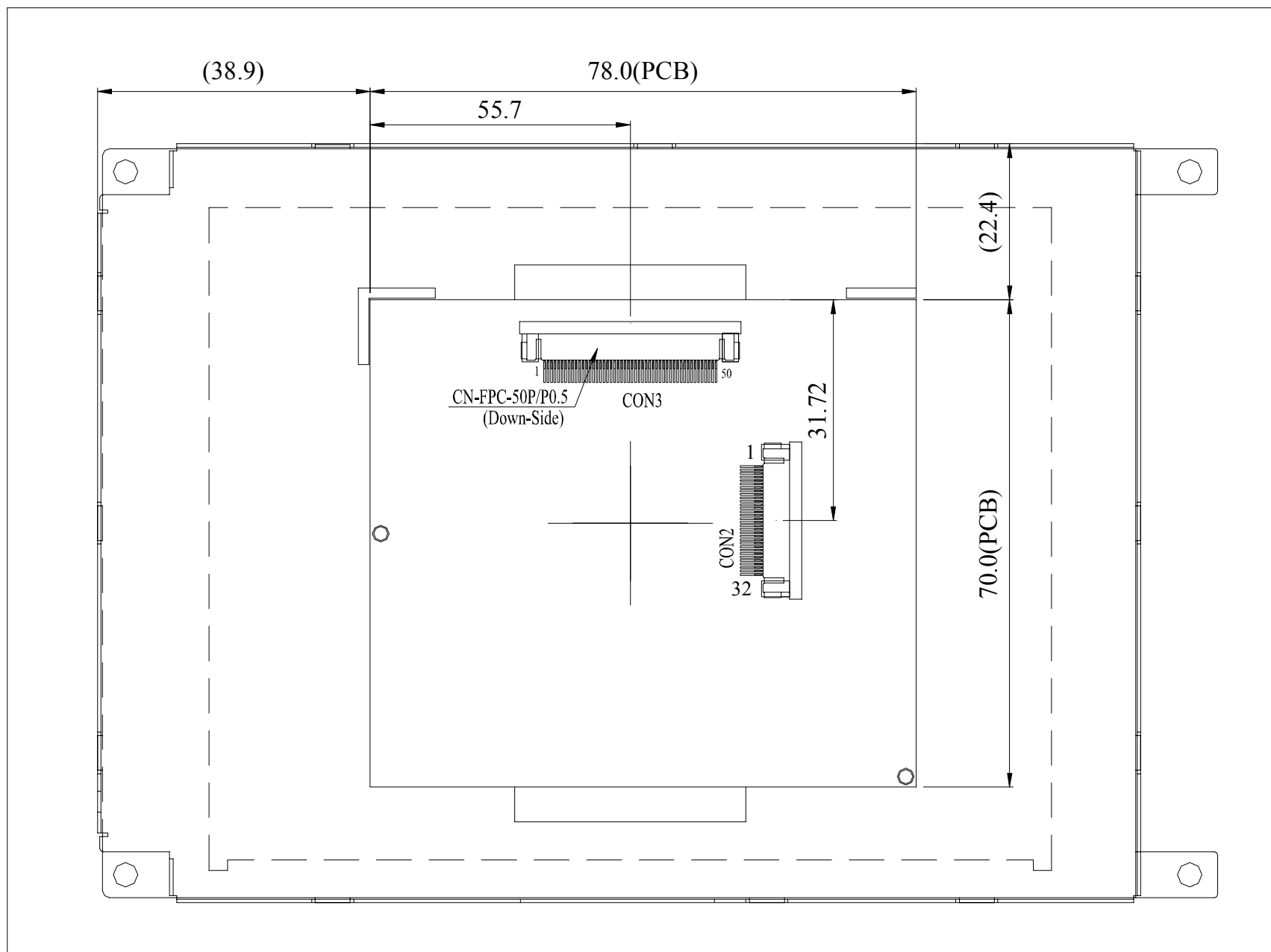
Color coordinates measured at the center point of LCD

Note 7: Measured at the center area of the panel when all the input terminals of LCD panel are electrically opened.

$$\text{Note 8 : Uniformity (U)} = \frac{\text{Brightness (min)}}{\text{Brightness (max)}} \times 100\%$$

11.Contour Drawing

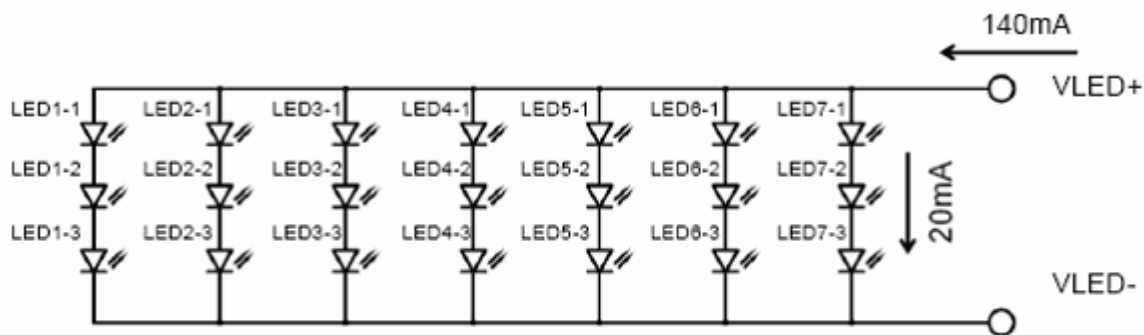




12. LED driving conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
LED Current	I_{LED}	----	140	210	mA	Note1
LED voltage	V_{LED}	9.0	10.2	10.5	V	
LED life Time	-	----	50K	----	-	Note 2,3,5
Luminous Intensity	IV	----	300	----	CD/M ²	Note 4

Note 1: There are 7 Groups LED shown as below, =9.9 V(Min)



Note 2 : $T_a = 25^{\circ}\text{C}$,

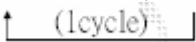
Note 3 : Brightness to be decreased to 50% of the initial value.

Note 4: The luminous is measured through LCD panel.

Note 5: 50K hours is only an estimate for reference.

13. Reliability Test

WIDE TEMPERATURE RELIABILITY TEST

N O.	ITEM	CONDITION			STANDARD	NOTE
1	High Temp. Storage	80°C	240 Hrs		Appearance without defect	
2	Low Temp. Storage	-30°C	240 Hrs		Appearance without defect	
3	High Temp. & High Humi. Storage	60 °C 90%RH	240 Hrs		Appearance without defect	
4	High Temp. Operating Display	70°C	240 Hrs		Appearance without defect	
5	Low Temp. Operating Display	-20°C	240 Hrs		Appearance without defect	
6	Thermal Shock	-20 °C , 30min. → 70°C , 30min. 			Appearance without defect	10 cycles

Inspection Provision

1.Purpose

The WINSTAR inspection provision provides outgoing inspection provision and its expected quality level based on our outgoing inspection of WINSTAR LCD produces.

2.Applicable Scope

The WINSTAR inspection provision is applicable to the arrangement in regard to outgoing inspection and quality assurance after outgoing.

3.Technical Terms

3-1 WINSTAR Technical Terms



4.Outgoing Inspection

4-1 Inspection Method

MIL-STD-105E Level II Regular inspection

4-2 Inspection Standard

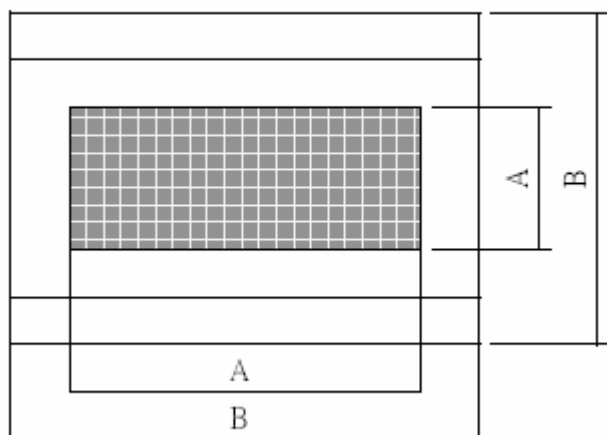
	Item		AQL(%)	Remarks
Major Defect	Dots	Opens Shorts Erroneous operation	0.4	Faults which substantially lower the practicality and the initial purpose difficult to achieve
	Solder appearance	Shorts Loose		
	Cracks	Display surface cracks		

	Dimensions	External from Dimensions	0.4	
Minor Defect	Inside the glass	Black spots	0.65	Faults which appear to pose almost no obstacle to the practicality, effective use, and operation
	Polarizing plate	Scratches, foreign Matter, air bubbles, and peeling		
	Dots	Pinhole, deformation		
	Color tone	Color unevenness		
	Solder appearance	Cold solder Solder projections		

4-3 Inspection Provisions

*Viewing Area Definition

Fig. 1



A : Zone Viewing Area

B : Zone Glass Plate Outline

*Inspection place to be 500 to 1000 lux illuminance uniformly without glaring.

The distance between luminous source(daylight fluorescent lamp and cool white fluorescent lamp) and sample to be 30 cm to 50 cm.

*Test and measurement are performed under the following conditions, unless otherwise specified.

Temperature $20 \pm 15^{\circ}\text{C}$

Humidity $65 \pm 20\%\text{R.H.}$

Pressure 860~1060hPa(mmbar)

In case of doubtful judgment, it is performed under the following conditions.

Temperature $20 \pm 2^{\circ}\text{C}$

Humidity $65 \pm 5\%\text{R.H.}$

Pressure 860~1060hPa(mmbar)

5.Specification for quality check

5-1-1 Electrical characteristics :

NO.	Item	Criterion
1	Non operational	Fail
2	Miss operating	Fail
3	Contrast irregular	Fail
4	Response time	Within Specified value

5-1-2 Components soldering :

Should be no defective soldering such as shorting, loose terminal cold solder, peeling of printed circuit board pattern, improper mounting position, etc.

5-2 Inspection Standard for TFT panel

5-2-1 The environmental condition of inspection :

The environmental condition and visual inspection shall be conducted as below.

(1) Ambient temperature : $25 \pm 5^{\circ}\text{C}$

(2) Humidity : 25~75% RH

(3) External appearance inspection shall be conducted by using a single 20W fluorescent lamp or equivalent illumination.

(4) Visual inspection on the operation condition for cosmetic shall be conducted at the distance 30cm or more between the LCD panels and eyes of inspector. The viewing angle shall be 90 degree to the front surface of display panel.

(5) Ambient Illumination : 300~500 Lux for external appearance inspection.

(6) Ambient Illumination : 100~200 Lux for light on inspection.

5-2-2 Inspection Criteria

(1) Definition of dot defect induced from the panel inside

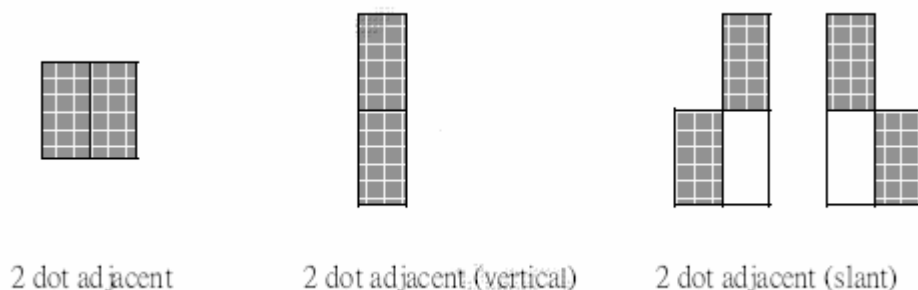
a) The definition of dot : The size of a defective dot over 1/2 of whole dot is regarded as one defective dot

b) Bright dot : Dots appear bright and unchanged in size in which LCD panel is displaying under black pattern.

c) Dark dot : Dots appear dark and unchanged in size in which LCD panel is displaying under pure red, green, blue pattern.

d) 2 dot adjacent = 1 pair = 2 dots

Picture :



(2) Display Inspection

NO.	Item		Acceptable Count
1	Dot defect	Bright Dot	Random $N \leq 2$
		2 dots adjacent	$N \leq 0$

		Dark Dot	Random	$N \leq 3$
			2 dots adjacent	$N \leq 1$
		Total bright and dark dot		$N \leq 4$
	Functional failure (V-line/ H-line/Cross line etc.)			Not allowable
	Mura	It's OK if mura is slight visible through 6% ND filter. (Judged by limit sample if it is necessary)		
2	Newton ring (touch panel)	Orbicular of interference fringes is not allowed in the optimum contrast within the active area under viewing angle.		

(3) Appearance inspection

NO.	Item	Standards
1	Panel Crack	Not allow. It is shown in Fig.1.
2	Broken CF Non -lead Side of TFT	The broken in the area of $W > 2\text{mm}$ is ignored, L is ignored. It is shown in Fig.2.
3	Broken Lead Side of TFT	FPC lead, electrical line or alignment mark can't be damaged. It is shown in Fig.3.
4	Broken Corner of TFT at Lead Side	FPC lead. electrical line or alignment mark can't be damaged. It is shown in Fig.4.
5	Burr of TFT / CF Edge	The distance of burr from the edge of TFT / CF, $W \leq 0.3\text{mm}$. It is shown in Fig.5.
6	Foreign Black / White/Bright Spot	(1) $0.15 < D \leq 0.5 \text{ mm}$, $N \leq 4$; (2) $D \leq 0.15\text{mm}$, Ignore. It is shown in Fig.6.
7	Foreign Black / White/Bright Line	(1) $0.05 < W \leq 0.1 \text{ mm}$, $0.3 < L \leq 2 \text{ mm}$, $N \leq 4$.
		(2) $W \leq 0.05\text{mm}$ and $L \leq 0.3\text{mm}$ Ignore.
		It is shown in Fig.7.
8	Color irregular	Not remarkable color irregular.

Fig 1.

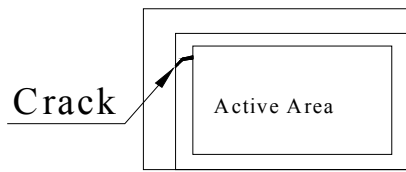


Fig 2.

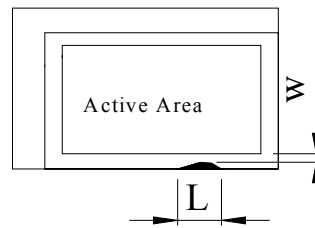


Fig 3.

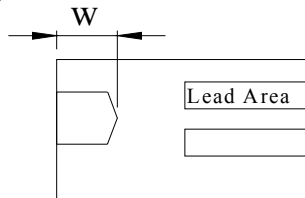


Fig 4.

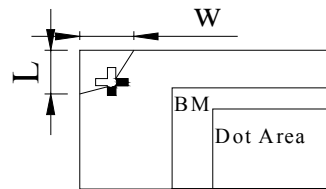


Fig 5.

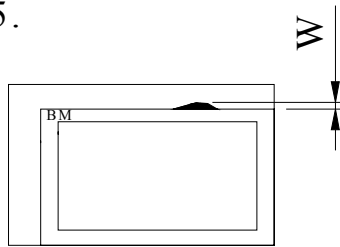
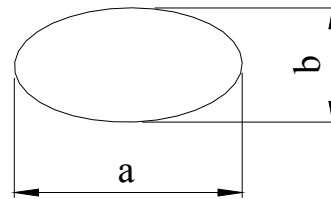


Fig 6.



$$D=(a+b)/2$$

Fig 7.

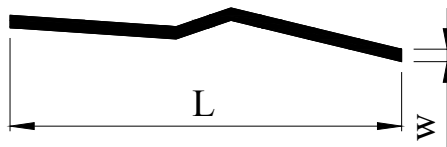
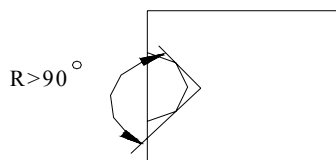


Fig8.



Notes

1.W:Width

2.Length

3.D:Average Diameter

4.N:Count

5.All the anhle of the broken must be larger than 90°.It is shown in Fig.8.(R>90°)

NOTICE:

• SAFETY

1. If the LCD panel breaks, be careful not to get the liquid crystal to touch your skin.
2. If the liquid crystal touches your skin or clothes, please wash it off immediately by using soap and water.

• HANDLING

1. Avoid static electricity which can damage the CMOS LSI.
2. Do not remove the panel or frame from the module.
3. The polarizing plate of the display is very fragile. So, please handle it very carefully.
4. Do not wipe the polarizing plate with a dry cloth, as it may easily scratch the surface of plate.
5. Do not use ketonics solvent & Aromatic solvent. Use a soft cloth soaked with a cleaning naphtha solvent.

• STORAGE

1. Store the panel or module in a dark place where the temperature is $25\pm 5^{\circ}\text{C}$ and the humidity is below 65% RH.
2. Do not place the module near organics solvents or corrosive gases.
3. Do not crush, shake, or jolt the module.

• TERMS OF WARRANT

1. Acceptance inspection period

The period is within one month after the arrival of contracted commodity at the buyer's factory site.

2. Applicable warrant period

The period is within twelve months since the date of shipping out under normal using and storage conditions.